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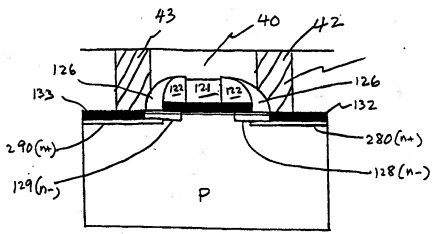
(54) Title: ULSI MOS WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR



(57) Abstract

MOS transistor formed on a semiconductor substrate of a first conductivity type and method of fabrication are provided. The device includes (a) an interfacial layer formed on the substrate; (b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r-(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s-(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t-(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u-(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of the second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer. The high dielectric layer can be subject to densification. The gate oxide material will significantly improve the performance of an MOS device by reducing or eliminating the current leakage associated with prior art devices.

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ULSI MOS WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR

Field of the Invention

The present invention relates generally to methods for fabricating integrated circuits using metal oxide semiconductor (MOS) technology. More particularly, the present invention relates to MOS devices with a gate width of less than 0.3 micron.

Background of the Invention

Metal oxide semiconductors are well known in the art. With the rapid integration of elements in the device, the thickness of the silicon oxide gate dielectric layer has approached the 2 nm thickness level. Such thin gate oxide layers require stringent protocols during fabrication especially in the gate etching process. In addition, concomitant with this reduction in the thickness of the gate oxide layer is the device's high leakage current caused by direct tunneling effects.

Shinriki et. al., U.S. Patent 5,292,673 describes a MOSFET that contains a tantalum pentoxide gate insulating film. Although the patent asserts that the device exhibits improved electrical characteristics, nevertheless, it is believed that the device suffers from, among other things, high leakage currents because of the silicon oxide layer, which is formed by reoxidation between the tantalum pentoxide gate insulating film and the silicon substrate, has defects including non-uniformity.

Summary of the Invention

The present invention is based in part on the recognition that employing a gate dielectric layer formed at least in part from a high dielectric constant material comprising Ta_2O_5 will significantly improve the performance of the MOS device by, among other things, reducing or eliminating the current leakage associated with prior art devices.

Accordingly, in one aspect the invention is directed to a method for fabricating an MOS device having a gate width of less than 0.3 micron that includes the steps of:

(a) forming an interfacial layer on a semiconductor substrate of a first conductive type wherein the interfacial is preferably sufficiently thin to limit parasitic capacitance of the device;

(b) forming a high dielectric constant layer on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) depositing a layer of electrically conductive material on the high dielectric constant layer;

(d) selectively removing portions of the layer of electrically conductive material to form a gate electrode and to expose portions of the high dielectric constant layer;

(e) implanting impurity ions through the exposed portions of the high dielectric constant layer into the substrate to form source and drain regions of a second conductive type;

(f) forming first spacers that are adjacent the gate electrode and cover portions of the source and drain regions of the second conductive type;

(g) removing the exposed portions of the high dielectric constant layer;

(h) implanting a second dose of impurity ions into the source and drain regions;

(i) depositing a layer of insulator material over the surface of the device, wherein the layer of insulator material may have an irregular surface;

(j) optionally, planarizing the surface of the insulator material;

(k) removing portions of the insulator material to form contact holes in the insulator material that are in communication with the source and drain regions; and

(l) filling the contact holes with contact material.

In preferred embodiments, the electrically conductive material comprises metal that is selected from the group consisting of TiN, W, Ta, Mo and mixtures thereof. Alternatively, the electrically conductive material comprises doped polysilicon.

In another embodiment the method includes the step of forming second spacers that are adjacent the first spacers and cover portions of the source and drain regions

following step (g) and before step (h) and/or the step of forming a silicide layer on the source and drain regions following step (h).

In another aspect, the invention is directed to an MOS transistor formed on a semiconductor substrate of a first conductivity type that includes:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of the second conductivity type; and

(f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

In a preferred embodiment, the MOS transistor also includes an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface.

Brief Description of the Drawings

Figures 1A through 1H illustrate the steps in fabricating an MOS device according to the present invention.

Detailed Description of the Preferred Embodiments

It is to be noted that "n+" and "n-" are used throughout the present disclosure. The short hand notation specifies the electron concentration of various regions of a metal-oxide-semiconductor device. For instance, "n-" specifies a region of light

electron concentration (on the order of $1 \times 10^{18} cm^{-3}$) while "n+" specifies a region of high electron concentration (on the order of $1 \times 10^{20} cm^{-3}$).

Figures 1A-1H illustrate an exemplary method for fabricating an integrated circuit device with the inventive process. A p type semiconductor substrate will be employed for illustrative purposes. Therefore, n- source and n- drain regions and n+source and n+ drain regions are formed in the substrate. Referring to Figure 1A, silicon substrate 100 has an interfacial layer 105 preferably comprising SiO_2, Si_3N_4, or silicon oxynitride formed on an upper surface of the substrate. The interfacial layer is formed by conventional processes, such as, for example, rapid thermal processing (RTP), thermal annealing, CVD, plasma nitridation or oxidation, or wet chemical treatment, such as immersion into boiling nitric acid. A preferred method of forming the interfacial layer comprises exposing the silicon substrate in an RF or microwave plasma in an atmosphere containing ozone, oxygen, N_2O, nitrogen, or mixtures thereof. The interfacial layer serves to prevent reaction of Ta_2O_5 in layer 110 with the silicon substrate. The interfacial layer will have a thickness that is sufficient to prevent reaction between the high dielectric constant layer and the silicon substrate and the thickness typically ranges from about 1 nm to 5 nm and preferably about 1 nm to 2 nm.

Subsequently, high dielectric constant layer 110 and electrically conductive layer 120 are formed on interfacial layer 105. The high dielectric constant layer 110 preferably comprises material that is selected from Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x preferably ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s preferably ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t preferably ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof. Typically, the high dielectric constant layer will have a thickness that ranges from about 4 nm to 12 nm and preferably from about 5 nm to 10 nm. The high dielectric constant layer will form the gate oxide layer. The particular high dielectric constant materials employed with the present invention allows for a thicker gate oxide layer to be formed, resulting in less stringent requirements on gate etching selectivity during the fabrication process. In addition, it is believed that during operation of the MOS transistors, the devices will exhibit a higher transconductance parameter. Further, since Ta has already been used in MOS fabrication, Ta_2O_5 containing gate oxides are expected to be compatible with

the materials in the other MOS materials. The high dielectric constant film can be fabricated by conventional means including, for example, LPCVD, PECVD, ECR CVD, UVCVD, and reactive sputtering.

In particular Ta_2O_5 films can be prepared by chemical vapor deposition (CVD) and physical vapor deposition (PVD) as described in Alers et al., "Nitrogen Plasma Annealing for Low Temperature Ta_2O_5 Films", Appl. Phys. Lett., Vol. 72, (11), March 1998, pages 1308-1310. $Ta_2(O_{1-x}N_x)_5$ films can be prepared by thermal CVD or plasma-assisted CVD as described in U.S. Patent 5,677,015. $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ films can be prepared by RF magnetron sputtering deposition as described in Gan et al. "Dielectric property of $(TiO_2)_x$ - $(Ta_2O_5)_{1-x}$ Thin Films", Appl. Phys. Lett. Vol. 72, (3), January 1998, pages 332-334 or by chemical CVD as described in U.S. Patent 4,734,340. $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ films can be prepared by metalorganic solution deposition as described in Joshi et al., "Structural and electrical properties of crystalline (1-x)Ta_2O_5-xAl_2O_3 thin films fabricated by metalorganic solution deposition technique", Appl. Phys. Lett. Vol. 71, (10), September 1997. Each of the above cited references is incorporated herein. Finally, the $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ and $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ thin films can be fabricated by techniques used in fabricating the other solid solution materials. Prior to formation of the electrically conductive layer 120, the high dielectric constant material is preferably subjected to a densification process comprising, for example, exposing the silicon substrate to a RTP or an RF or microwave plasma in an atmosphere containing ozone, oxygen, N_2O, nitrogen, or mixtures thereof. Densification is further described in Alers et. al. cited above. Densification improves the high dielectric constant material with respect to the leakage current of the MOS device made.

Electrically conductive layer 120 preferably comprises one or more layers of a high melting metal such as, for example, TiN, W, Ta, Mo which can be deposited by sputtering. This layer typically has a thickness that ranges from about 100 nm to 300 nm, and preferably from about 150 nm to 250 nm. As will be described herein, this electrically conductive layer will form the gate electrode in this embodiment.

An optional oxide layer can be deposited and patterned over the electrically conductive layer 120. Subsequently, a layer of photoresist material 160 is applied onto electrically conductive layer 120 before the photoresist is masked and patterned using conventional photoresist techniques to form a gate pattern. After etching, the line width (L) of the gate 121 is typically less than 0.3 micron, and preferably equal to or less than

about 0.18 micron. Etching down to the top high dielectric constant layer 110 removes the exposed electrically conductive material as shown in Figure 1B. Source 190 and drain 180 regions are formed by self aligned ion implantation before the remaining photoresist material 160A is removed to form the device shown in Figure 1C. As is apparent, interfacial layer 105 shown in Figures 1A and 1B is not shown in Figure 1C or subsequent figures although the layer is present in the structures illustrated.

Referring to Figure 1D, spacers 122 are formed by depositing a phosphosilicate glass (PSG) film 124 over the entire surface of the device of Figure 1C and then anisotropic etching the glass. The spacers can also be made from oxides or nitrides. Subsequently, the exposed high dielectric constant material is removed by plasma etching using fluorine or chlorine containing etchant gases to yield the structure of Figure 1E. The remaining layer of high dielectric material 115 serves as the gate oxide. Second spacers 126 are formed by the same procedure as for spacers 122. Lightly doped source (n-) 129 and drain (n-) 128 regions are then formed by ion implantation as shown in Figure 1F with the concomitant formation of source (n+) 290 and drain (n+) 280 regions.

Silicide layers 133 and 132 are then formed on the source and drain regions. One method comprises the steps of (1) depositing a layer of suitable metal preferably titanium, cobalt, or multiple layers of these metals, over the surface of the device of Figure 1F, (2) allowing the metal and silicon in the substrate to react, and thereafter (3) removing unreacted metal. Another method comprises depositing silicide, e.g., $metal_xSi_y$, directly onto source and drain regions using conventional selective deposition techniques, e.g., CVD.

Following formation of the silicide regions, a conformal layer of PSG film 40 is deposited on the structure of Figure 1G, thereafter, the top surface of the PSG film is planarized by conventional techniques such as chemical-mechanical polishing (CMP). CMP is particularly advantageous when small contact holes (less than 0.3 micron) are required. Subsequently, contact holes are etched in the PSG and they then filled with an electrically conductive, e.g., metal, material 42 and 43 as shown in Fig. 1H.

As is apparent, the above structure has a metal gate electrode 121. In an alternative embodiment, instead of a metal gate electrode, a doped polysilicon gate electrode can be employed. In this case, a doped polysilicon layer would be deposited in place of the electrically conductive 120 layer as shown in Figure 1A. Optionally, a

diffusion barrier layer made from a suitable material such as, for example, TiN, WN, and TaN, can be deposited between layers 110 and 120. This barrier layer, which is typically 5 nm to 15 nm thick, prevents polysilicon gate material from reacting with the tantalum pentoxide in the gate dielectric. In this scenario, the rest of the process would be essentially the same as above, however, the preferred silicidation procedure entails depositing a metal film over the structure so that a polycide layer on the surface of the doped polysilicon layer is formed as well.

It is to be emphasized that although n channel transistors have been described in detail herein, the present invention may also be practiced as a p channel transistor. In fabricating the p channel device, the doping conductives of the p channel device are simply opposite to those of the n channel device.

Although only preferred embodiments of the invention are specifically disclosed and described above, it will be appreciated that many modifications and variations of the present invention are possible in light of the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.

CLAIMS:

1. A method for fabricating a MOS device having a gate width of less than 0.3 micron that comprises the steps of:

(a) forming an interfacial layer on a semiconductor substrate of a first conductivity type;

(b) forming a high dielectric constant layer on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) depositing a layer of electrically conductive material on the high dielectric constant layer;

(d) selectively removing portions of the layer of electrically conductive material to form a gate electrode and to expose portions of the high dielectric constant layer;

(e) implanting impurity ions through the exposed portions of the high dielectric constant layer into the substrate to form source and drain regions of a second conductivity type;

(f) forming first spacers that are adjacent the gate electrode and cover portions of the source and drain regions of the second conductivity type;

(g) removing the exposed portions of the high dielectric constant layer;

(h) implanting a second dose of impurity ions into the source and drain regions;

(i) depositing a layer of insulator material over the surface of the device;

(j) optionally, planarizing the surface of the insulator material;

(k) removing portions of the insulator material to form contact holes in the insulator material that are in communication with the source and drain regions; and

(l) filling the contact holes with contact material.

2. The method of claim 1 comprising the step of densifying the high dielectric constant layer.

3. The method of claim 1 wherein the electrically conductive material comprises metal that is selected from the group consisting of TiN, W, Ta, Mo and multilayers thereof.

4. The method of claim 1 wherein the electrically conductive material comprises doped polysilicon.

5. The method of claim 4 further comprising the step of forming a barrier layer between the electrically conductive material and the high dielectric constant layer.

6. The method of claim 1 further comprising the step of forming second spacers that are adjacent the first spacers and cover portions of the source and drain regions following step (g) and before step (h).

7. The method of claim 1 further comprising the step of forming a silicide layer on the source and drain regions following step (h).

8. The method of claim 7 wherein forming the silicide layer comprises the steps of:

depositing a layer of metal over the at least the source and drain regions;

heating the layer of metal to cause the metal to react with the silicon on the surface of the source and drain regions to form metal silicide layers in the source and drain regions; and

removing unreacted metal from the layer of metal.

9. The method of claim 7 wherein forming the silicide layer comprises selectively depositing silicide over the source and drain regions.

10. The method of claim 1 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

11. The method of claim 1 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

12. The method of claim 1 wherein step (h) comprises introducing a light dosage of impurities to form lightly doped source and drain regions.

13. The method of claim 1 wherein the high dielectric constant material is Ta_2O_5.

14. The method of claim 1 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6.

15. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1.

16. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1.

17. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1.

18. The method of claim 1 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1.

19. The method of claim 1 wherein the substrate comprises silicon.

20. The method of claim 1 wherein the first spacers comprise an oxide or nitride material.

21. The method of claim 1 wherein step (i) comprises depositing a conformal layer of insulator material and (j) planarizes the surface of the insulator material by chemical mechanical planarization.

22. An MOS transistor formed on a semiconductor substrate of a first conductivity type comprising:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of a second conductivity type; and

(f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

23. The MOS transistor of claim 22 comprising:

(g) an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface.

24. The MOS transistor of claim 22 wherein the gate electrode is formed from a metal that is selected from the group consisting of TiN, W, Ta, MO and multilayers thereof.

25. The MOS transistor claim 22 wherein the gate electrode comprises doped polysilicon.

26. The MOS transistor of claim 25 comprising a barrier layer between the gate electrode and the high dielectric constant layer.

27. The MOS transistor of claim 22 comprising a pair of second spacers that are adjacent to the first spacers and formed on the lightly doped regions.

28. The MOS transistor of claim 22 comprising a silicide layer on the source and drain regions.

29. The MOS transistor of claim 22 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

30. The MOS transistor of claim 22 wherein the high dielectric constant material is Ta_2O_5.

31. The MOS transistor of claim 22 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from 0 to 0.6.

32. The MOS transistor of claim 22 herein the high dielectric constant material is a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1.

33. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1.

34. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1.

35. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1.

36. The MOS transistor of claim 22 wherein the substrate comprises silicon.

37. The MOS transistor of claim 22 wherein the first spacers comprise an oxide or nitride material.

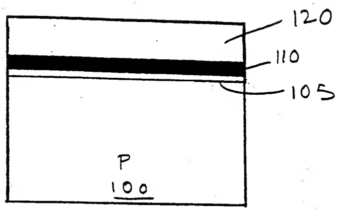

FIG. 1A

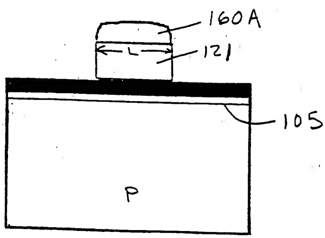

FIG. 1B

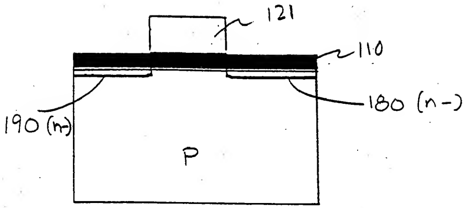

FIG. 1C

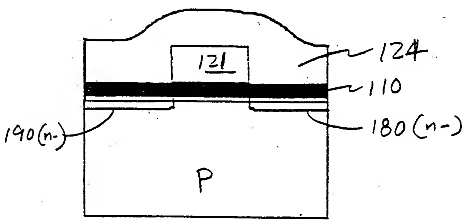

FIG. 1D

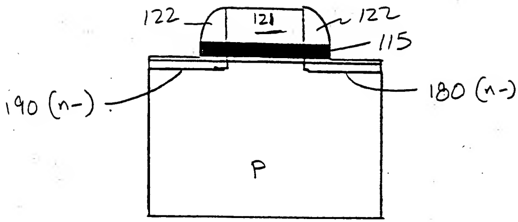
122
121
122
115
190 (n-)
180 (n-)
P

FIG. 1E

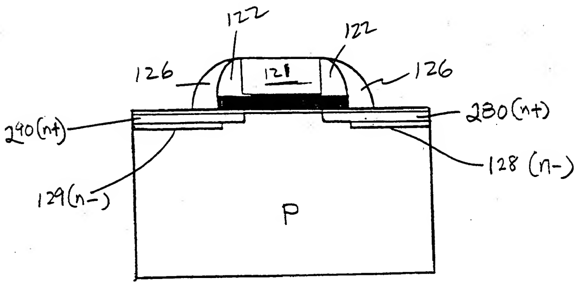
122
122
126
121
126
240(n+)
280(n+)
128 (n-)
129(n-)
P

FIG. 1F

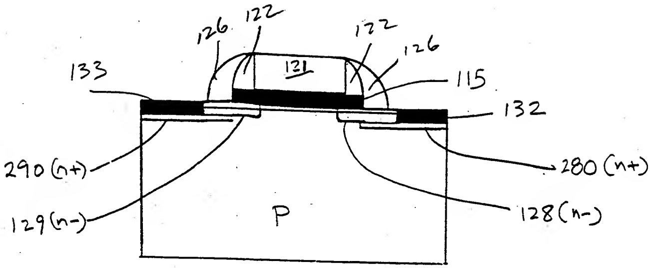
126
122
122
126
121
133
115
132
290 (n+)
280 (n+)
129 (n-)
128 (n-)
P

FIG. 1G

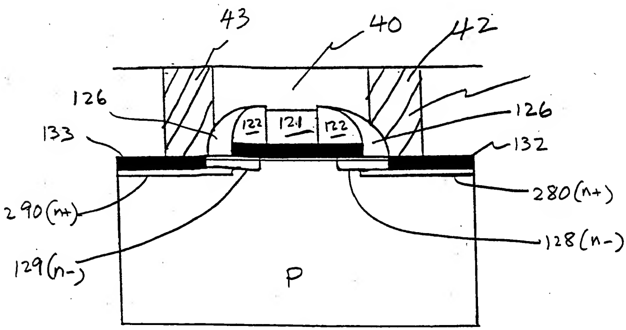
43
40
42
126
126
122
121
122
133
132
290 (n+)
280 (n+)
128 (n-)
129 (n-)
P

FIG. 1H

International Application No
PCT/US 99/13787

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/336 H01L29/51 H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 292 673 A (SHINRIKI HIROSHI ET AL) 8 March 1994 (1994-03-08) cited in the application figures 6-9 column 2, line 3 - line 9 column 3, line 41 -column 4, line 5 column 4, line 25 - line 65 column 5, line 9 - line 11 column 5, line 22 -column 7, line 19	22, 24-27, 29,30, 36,37
A		1,3-6, 10,11, 13,19,20

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[X] Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
30 September 1999	15/10/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Polesello, P

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/13787

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Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
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A	EP 0 844 647 A (TEXAS INSTRUMENTS INC) 27 May 1998 (1998-05-27) figure 2 column 2, line 7 - line 12 column 2, line 50 -column 3, line 54 ---	1,4,5, 10-12, 19,20, 22,25, 26,36,37
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A	US 5 702 972 A (HSU SHUN-LIANG ET AL) 30 December 1997 (1997-12-30) figures 2-7,9 column 2, line 35 -column 4, line 4 ---	1,4,6-9, 11,12, 19-23, 25,27, 28,36,37
A	US 5 688 724 A (YOON EUISIK ET AL) 18 November 1997 (1997-11-18) figures 1-6 column 3, line 63 -column 6, line 18 ---	1-5,11, 13,19
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
A	REDDY P K ET AL: "Dielectric properties of tantalum oxynitride films. (Thin film capacitors for hybrid integrated circuits)" PHYSICA STATUS SOLIDI A, 16 JULY 1979, EAST GERMANY, vol. 54, no. 1, pages K63-K66, XP002117111 ISSN: 0031-8965 page K63, line 23 -page K65, line 16 figure 2 ---	1,14,22, 31
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/13787

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(74) Agent: PETERSON, James, W.; Burns, Doane, Swecker & Mathis, L.L.P., P.O. Box 1404, Alexandria, VA 22313–1404 (US).

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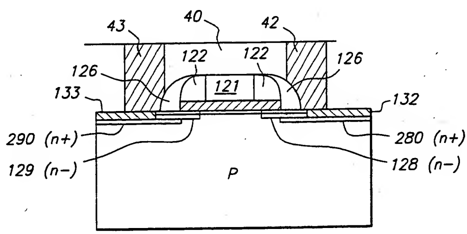
(54) Title: ULSI MOS WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR



(57) Abstract

MOS transistor formed on a semiconductor substrate of a first conductivity type and method of fabrication are provided. The device includes (a) an interfacial layer formed on the substrate; (b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r-(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s-(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t-(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u-(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of the second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer. The high dielectric layer can be subject to densification. The gate oxide material will significantly improve the performance of an MOS device by reducing or eliminating the current leakage associated with prior art devices.

*(Referred to in PCT Gazette No. 13/2000, Section II)

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ULSI MOS WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR

Field of the Invention

The present invention relates generally to methods for fabricating integrated circuits using metal oxide semiconductor (MOS) technology. More particularly, the present invention relates to MOS devices with a gate width of less than 0.3 micron.

Background of the Invention

Metal oxide semiconductors are well known in the art. With the rapid integration of elements in the device, the thickness of the silicon oxide gate dielectric layer has approached the 2 nm thickness level. Such thin gate oxide layers require stringent protocols during fabrication especially in the gate etching process. In addition, concomitant with this reduction in the thickness of the gate oxide layer is the device's high leakage current caused by direct tunneling effects.

Shinriki et. al., U.S. Patent 5,292,673 describes a MOSFET that contains a tantalum pentoxide gate insulating film. Although the patent asserts that the device exhibits improved electrical characteristics, nevertheless, it is believed that the device suffers from, among other things, high leakage currents because of the silicon oxide layer, which is formed by reoxidation between the tantalum pentoxide gate insulating film and the silicon substrate, has defects including non-uniformity.

Summary of the Invention

The present invention is based in part on the recognition that employing a gate dielectric layer formed at least in part from a high dielectric constant material comprising Ta_2O_5 will significantly improve the performance of the MOS device by, among other things, reducing or eliminating the current leakage associated with prior art devices.

Accordingly, in one aspect the invention is directed to a method for fabricating an MOS device having a gate width of less than 0.3 micron that includes the steps of:

(a) forming an interfacial layer on a semiconductor substrate of a first conductive type wherein the interfacial is preferably sufficiently thin to limit parasitic capacitance of the device;

(b) forming a high dielectric constant layer on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) depositing a layer of electrically conductive material on the high dielectric constant layer;

(d) selectively removing portions of the layer of electrically conductive material to form a gate electrode and to expose portions of the high dielectric constant layer;

(e) implanting impurity ions through the exposed portions of the high dielectric constant layer into the substrate to form source and drain regions of a second conductive type;

(f) forming first spacers that are adjacent the gate electrode and cover portions of the source and drain regions of the second conductive type;

(g) removing the exposed portions of the high dielectric constant layer;

(h) implanting a second dose of impurity ions into the source and drain regions;

(i) depositing a layer of insulator material over the surface of the device, wherein the layer of insulator material may have an irregular surface;

(j) optionally, planarizing the surface of the insulator material;

(k) removing portions of the insulator material to form contact holes in the insulator material that are in communication with the source and drain regions; and

(l) filling the contact holes with contact material.

In preferred embodiments, the electrically conductive material comprises metal that is selected from the group consisting of TiN, W, Ta, Mo and mixtures thereof. Alternatively, the electrically conductive material comprises doped polysilicon.

In another embodiment the method includes the step of forming second spacers that are adjacent the first spacers and cover portions of the source and drain regions

following step (g) and before step (h) and/or the step of forming a silicide layer on the source and drain regions following step (h).

In another aspect, the invention is directed to an MOS transistor formed on a semiconductor substrate of a first conductivity type that includes:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of the second conductivity type; and

(f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

In a preferred embodiment, the MOS transistor also includes an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface.

Brief Description of the Drawings

Figures 1A through 1H illustrate the steps in fabricating an MOS device according to the present invention.

Detailed Description of the Preferred Embodiments

It is to be noted that "n+" and "n-" are used throughout the present disclosure. The short hand notation specifies the electron concentration of various regions of a metal-oxide-semiconductor device. For instance, "n-" specifies a region of light

electron concentration (on the order of $1x10^{18}cm^{-3}$) while "n+" specifies a region of high electron concentration (on the order of $1x10^{20}cm^{-3}$).

Figures 1A-1H illustrate an exemplary method for fabricating an integrated circuit device with the inventive process. A p type semiconductor substrate will be employed for illustrative purposes. Therefore, n- source and n- drain regions and n+source and n+ drain regions are formed in the substrate. Referring to Figure 1A, silicon substrate 100 has an interfacial layer 105 preferably comprising SiO_2, Si_3N_4, or silicon oxynitride formed on an upper surface of the substrate. The interfacial layer is formed by conventional processes, such as, for example, rapid thermal processing (RTP), thermal annealing, CVD, plasma nitridation or oxidation, or wet chemical treatment, such as immersion into boiling nitric acid. A preferred method of forming the interfacial layer comprises exposing the silicon substrate in an RF or microwave plasma in an atmosphere containing ozone, oxygen, N_2O, nitrogen, or mixtures thereof. The interfacial layer serves to prevent reaction of Ta_2O_5 in layer 110 with the silicon substrate. The interfacial layer will have a thickness that is sufficient to prevent reaction between the high dielectric constant layer and the silicon substrate and the thickness typically ranges from about 1 nm to 5 nm and preferably about 1 nm to 2 nm.

Subsequently, high dielectric constant layer 110 and electrically conductive layer 120 are formed on interfacial layer 105. The high dielectric constant layer 110 preferably comprises material that is selected from Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x preferably ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s preferably ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t preferably ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof. Typically, the high dielectric constant layer will have a thickness that ranges from about 4 nm to 12 nm and preferably from about 5 nm to 10 nm. The high dielectric constant layer will form the gate oxide layer. The particular high dielectric constant materials employed with the present invention allows for a thicker gate oxide layer to be formed, resulting in less stringent requirements on gate etching selectivity during the fabrication process. In addition, it is believed that during operation of the MOS transistors, the devices will exhibit a higher transconductance parameter. Further, since Ta has already been used in MOS fabrication, Ta_2O_5 containing gate oxides are expected to be compatible with

the materials in the other MOS materials. The high dielectric constant film can be fabricated by conventional means including, for example, LPCVD, PECVD, ECR CVD, UVCVD, and reactive sputtering.

In particular Ta_2O_5 films can be prepared by chemical vapor deposition (CVD) and physical vapor deposition (PVD) as described in Alers et al., "Nitrogen Plasma Annealing for Low Temperature Ta_2O_5 Films", Appl. Phys. Lett., Vol. 72, (11), March 1998, pages 1308-1310. $Ta_2(O_{1-x}N_x)_5$ films can be prepared by thermal CVD or plasma-assisted CVD as described in U.S. Patent 5,677,015. $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ films can be prepared by RF magnetron sputtering deposition as described in Gan et al. "Dielectric property of $(TiO_2)_x$ - $(Ta_2O_5)_{1-x}$ Thin Films", Appl. Phys. Lett. Vol. 72, (3), January 1998, pages 332-334 or by chemical CVD as described in U.S. Patent 4,734,340. $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ films can be prepared by metalorganic solution deposition as described in Joshi et al., "Structural and electrical properties of crystalline (1-x)Ta_2O_5-xAl_2O_3 thin films fabricated by metalorganic solution deposition technique", Appl. Phys. Lett. Vol. 71, (10), September 1997. Each of the above cited references is incorporated herein. Finally, the $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ and $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ thin films can be fabricated by techniques used in fabricating the other solid solution materials. Prior to formation of the electrically conductive layer 120, the high dielectric constant material is preferably subjected to a densification process comprising, for example, exposing the silicon substrate to a RTP or an RF or microwave plasma in an atmosphere containing ozone, oxygen, N_2O, nitrogen, or mixtures thereof. Densification is further described in Alers et. al. cited above. Densification improves the high dielectric constant material with respect to the leakage current of the MOS device made.

Electrically conductive layer 120 preferably comprises one or more layers of a high melting metal such as, for example, TiN, W, Ta, Mo which can be deposited by sputtering. This layer typically has a thickness that ranges from about 100 nm to 300 nm, and preferably from about 150 nm to 250 nm. As will be described herein, this electrically conductive layer will form the gate electrode in this embodiment.

An optional oxide layer can be deposited and patterned over the electrically conductive layer 120. Subsequently, a layer of photoresist material 160 is applied onto electrically conductive layer 120 before the photoresist is masked and patterned using conventional photoresist techniques to form a gate pattern. After etching, the line width (L) of the gate 121 is typically less than 0.3 micron, and preferably equal to or less than

about 0.18 micron. Etching down to the top high dielectric constant layer 110 removes the exposed electrically conductive material as shown in Figure 1B. Source 190 and drain 180 regions are formed by self aligned ion implantation before the remaining photoresist material 160A is removed to form the device shown in Figure 1C. As is apparent, interfacial layer 105 shown in Figures 1A and 1B is not shown in Figure 1C or subsequent figures although the layer is present in the structures illustrated.

Referring to Figure 1D, spacers 122 are formed by depositing a phosphosilicate glass (PSG) film 124 over the entire surface of the device of Figure 1C and then anisotropic etching the glass. The spacers can also be made from oxides or nitrides. Subsequently, the exposed high dielectric constant material is removed by plasma etching using fluorine or chlorine containing etchant gases to yield the structure of Figure 1E. The remaining layer of high dielectric material 115 serves as the gate oxide. Second spacers 126 are formed by the same procedure as for spacers 122. Lightly doped source (n-) 129 and drain (n-) 128 regions are then formed by ion implantation as shown in Figure 1F with the concomitant formation of source (n+) 290 and drain (n+) 280 regions.

Silicide layers 133 and 132 are then formed on the source and drain regions. One method comprises the steps of (1) depositing a layer of suitable metal preferably titanium, cobalt, or multiple layers of these metals, over the surface of the device of Figure 1F, (2) allowing the metal and silicon in the substrate to react, and thereafter (3) removing unreacted metal. Another method comprises depositing silicide, e.g., $metal_xSi_y$, directly onto source and drain regions using conventional selective deposition techniques, e.g., CVD.

Following formation of the silicide regions, a conformal layer of PSG film 40 is deposited on the structure of Figure 1G, thereafter, the top surface of the PSG film is planarized by conventional techniques such as chemical-mechanical polishing (CMP). CMP is particularly advantageous when small contact holes (less than 0.3 micron) are required. Subsequently, contact holes are etched in the PSG and they then filled with an electrically conductive, e.g., metal, material 42 and 43 as shown in Fig. 1H.

As is apparent, the above structure has a metal gate electrode 121. In an alternative embodiment, instead of a metal gate electrode, a doped polysilicon gate electrode can be employed. In this case, a doped polysilicon layer would be deposited in place of the electrically conductive 120 layer as shown in Figure 1A. Optionally, a

diffusion barrier layer made from a suitable material such as, for example, TiN, WN, and TaN, can be deposited between layers 110 and 120. This barrier layer, which is typically 5 nm to 15 nm thick, prevents polysilicon gate material from reacting with the tantalum pentoxide in the gate dielectric. In this scenario, the rest of the process would be essentially the same as above, however, the preferred silicidation procedure entails depositing a metal film over the structure so that a polycide layer on the surface of the doped polysilicon layer is formed as well.

It is to be emphasized that although n channel transistors have been described in detail herein, the present invention may also be practiced as a p channel transistor. In fabricating the p channel device, the doping conductives of the p channel device are simply opposite to those of the n channel device.

Although only preferred embodiments of the invention are specifically disclosed and described above, it will be appreciated that many modifications and variations of the present invention are possible in light of the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.

CLAIMS:

1. A method for fabricating a MOS device having a gate width of less than 0.3 micron that comprises the steps of:

(a) forming an interfacial layer on a semiconductor substrate of a first conductivity type;

(b) forming a high dielectric constant layer on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) depositing a layer of electrically conductive material on the high dielectric constant layer;

(d) selectively removing portions of the layer of electrically conductive material to form a gate electrode and to expose portions of the high dielectric constant layer;

(e) implanting impurity ions through the exposed portions of the high dielectric constant layer into the substrate to form source and drain regions of a second conductivity type;

(f) forming first spacers that are adjacent the gate electrode and cover portions of the source and drain regions of the second conductivity type;

(g) removing the exposed portions of the high dielectric constant layer;

(h) implanting a second dose of impurity ions into the source and drain regions;

(i) depositing a layer of insulator material over the surface of the device;

(j) optionally, planarizing the surface of the insulator material;

(k) removing portions of the insulator material to form contact holes in the insulator material that are in communication with the source and drain regions; and

(l) filling the contact holes with contact material.

2. The method of claim 1 comprising the step of densifying the high dielectric constant layer.

3. The method of claim 1 wherein the electrically conductive material comprises metal that is selected from the group consisting of TiN, W, Ta, Mo and multilayers thereof.

4. The method of claim 1 wherein the electrically conductive material comprises doped polysilicon.

5. The method of claim 4 further comprising the step of forming a barrier layer between the electrically conductive material and the high dielectric constant layer.

6. The method of claim 1 further comprising the step of forming second spacers that are adjacent the first spacers and cover portions of the source and drain regions following step (g) and before step (h).

7. The method of claim 1 further comprising the step of forming a silicide layer on the source and drain regions following step (h).

8. The method of claim 7 wherein forming the silicide layer comprises the steps of:

depositing a layer of metal over the at least the source and drain regions;

heating the layer of metal to cause the metal to react with the silicon on the surface of the source and drain regions to form metal silicide layers in the source and drain regions; and

removing unreacted metal from the layer of metal.

9. The method of claim 7 wherein forming the silicide layer comprises selectively depositing silicide over the source and drain regions.

10. The method of claim 1 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

11. The method of claim 1 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

12. The method of claim 1 wherein step (h) comprises introducing a light dosage of impurities to form lightly doped source and drain regions.

13. The method of claim 1 wherein the high dielectric constant material is Ta_2O_5.

14. The method of claim 1 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6.

15. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1.

16. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1.

17. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1.

18. The method of claim 1 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1.

19. The method of claim 1 wherein the substrate comprises silicon.

20. The method of claim 1 wherein the first spacers comprise an oxide or nitride material.

21. The method of claim 1 wherein step (i) comprises depositing a conformal layer of insulator material and (j) planarizes the surface of the insulator material by chemical mechanical planarization.

22. An MOS transistor formed on a semiconductor substrate of a first conductivity type comprising:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of a second conductivity type; and

(f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

23. The MOS transistor of claim 22 comprising:

(g) an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface.

24. The MOS transistor of claim 22 wherein the gate electrode is formed from a metal that is selected from the group consisting of TiN, W, Ta, MO and multilayers thereof.

25. The MOS transistor claim 22 wherein the gate electrode comprises doped polysilicon.

26. The MOS transistor of claim 25 comprising a barrier layer between the gate electrode and the high dielectric constant layer.

27. The MOS transistor of claim 22 comprising a pair of second spacers that are adjacent to the first spacers and formed on the lightly doped regions.

28. The MOS transistor of claim 22 comprising a silicide layer on the source and drain regions.

29. The MOS transistor of claim 22 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

30. The MOS transistor of claim 22 wherein the high dielectric constant material is Ta_2O_5.

31. The MOS transistor of claim 22 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from 0 to 0.6.

32. The MOS transistor of claim 22 herein the high dielectric constant material is a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1.

33. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1.

34. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1.

35. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1.

36. The MOS transistor of claim 22 wherein the substrate comprises silicon.

37. The MOS transistor of claim 22 wherein the first spacers comprise an oxide or nitride material.

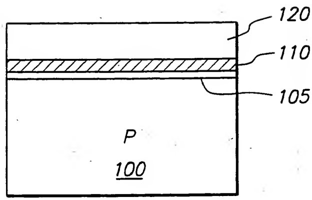


FIG. 1A

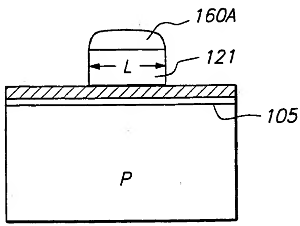


FIG. 1B

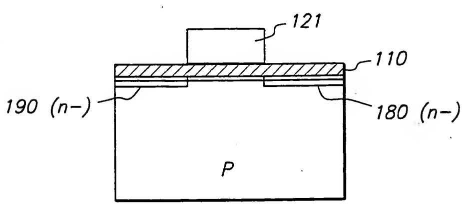


FIG. 1C

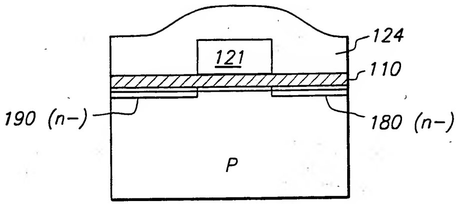


FIG. 1D

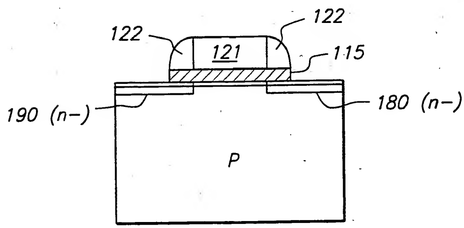


FIG. 1E

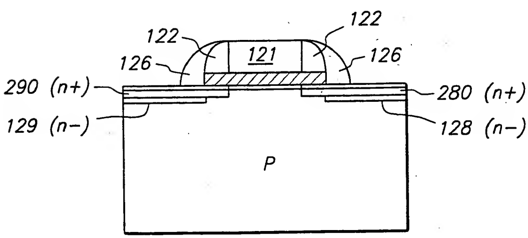
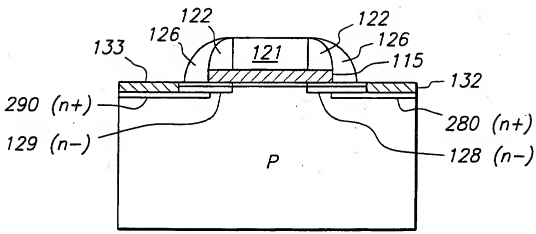


FIG. 1F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133
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132
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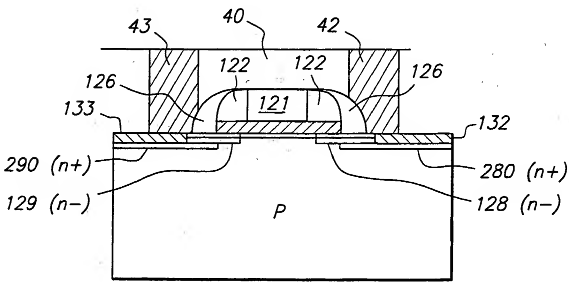
280 (n+)
129 (n-)
128 (n-)
P

FIG. 1G


43
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126
133
121
132
290 (n+)
280 (n+)
129 (n-)
128 (n-)
P

FIH. 1H

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/13787

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/336 H01L29/51 H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 292 673 A (SHINRIKI HIROSHI ET AL) 8 March 1994 (1994-03-08) cited in the application figures 6-9 column 2, line 3 - line 9 column 3, line 41 -column 4, line 5 column 4, line 25 - line 65 column 5, line 9 - line 11 column 5, line 22 -column 7, line 19	22, 24-27, 29,30, 36,37
A		1,3-6, 10,11, 13,19,20

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 September 1999	15/10/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Polesello, P

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Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	PATENT ABSTRACTS OF JAPAN vol. 098, no. 011, 30 September 1998 (1998-09-30) -& JP 10 178170 A (FUJITSU LTD), 30 June 1998 (1998-06-30)	22,30,36
P,A	abstract; figures 1-6	1,11,13, 19

A	EP 0 844 647 A (TEXAS INSTRUMENTS INC) 27 May 1998 (1998-05-27) figure 2 column 2, line 7 - line 12 column 2, line 50 -column 3, line 54	1,4,5, 10-12, 19,20, 22,25, 26,36,37

A	US 5 596 214 A (ENDO NOBUHIRO) 21 January 1997 (1997-01-21) figures 3,5,7,9 column 14, line 48 -column 15, line 27 column 16, line 63 -column 17, line 11 column 18, line 45 -column 19, line 12	1,3,11, 13,19, 22-24, 30,36

A	US 3 731 163 A (SHUSKUS A) 1 May 1973 (1973-05-01) figure 1 column 3, line 61 -column 4, line 30	1-4,11, 13-19, 22,24, 25,30-36

A	US 5 702 972 A (HSU SHUN-LIANG ET AL) 30 December 1997 (1997-12-30) figures 2-7,9 column 2, line 35 -column 4, line 4	1,4,6-9, 11,12, 19-23, 25,27, 28,36,37

A	US 5 688 724 A (YOON EUISIK ET AL) 18 November 1997 (1997-11-18) figures 1-6 column 3, line 63 -column 6, line 18	1-5,11, 13,19

A	PRATT I H: "Thin-film dielectric properties of r.f. sputtered oxides" SOLID STATE TECHNOLOGY, DEC. 1969, USA, vol. 12, no. 12, pages 49-57, XP002117110 ISSN: 0038-111X page 53, column 2, line 5 -page 55, column 2, line 28 tables II-III figure 10	1,13,16, 18,22, 30,33,35

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	REDDY P K ET AL: "Dielectric properties of tantalum oxynitride films. (Thin film capacitors for hybrid integrated circuits)" PHYSICA STATUS SOLIDI A, 16 JULY 1979, EAST GERMANY, vol. 54, no. 1, pages K63-K66, XP002117111 ISSN: 0031-8965 page K63, line 23 -page K65, line 16 figure 2 ---	1,14,22, 31
A	GAN J -Y ET AL: "Dielectric property of (TiO/sub 2/)/sub x/-(Ta/sub 2/O/sub 5/)/sub 1-x/ thin films" APPLIED PHYSICS LETTERS, 19 JAN. 1998, AIP, USA, vol. 72, no. 3, pages 332-334, XP002116551 ISSN: 0003-6951 cited in the application * the whole document * ---	1,2,15, 22,31
A	JOSHI P C ET AL: "Structural and electrical properties of crystalline (1-x)Ta/sub 2/O/sub 5/-xAl/sub 2/O/sub 3/ thin films fabricated by metalorganic solution deposition technique" APPLIED PHYSICS LETTERS, 8 SEPT. 1997, AIP, USA, vol. 71, no. 10, pages 1341-1343, XP002116552 ISSN: 0003-6951 cited in the application abstract page 1343, column 2, line 9 - line 16 page 1343, column 2, line 23 - line 27 ---	1,16,22, 33
A	VLASOV Y G ET AL: "Analytical applications of pH-ISFETs" SENSORS AND ACTUATORS B (CHEMICAL), DEC. 1992, SWITZERLAND, vol. B10, no. 1, pages 1-6, XP002117112 ISSN: 0925-4005 page 1, column 1, line 17 - line 25 ---	1,17,19, 22,34,36

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In' national Application No
PCT/US 99/13787

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ALERS G B ET AL: "Nitrogen plasma annealing for low temperature Ta/sub 2/O/sub 5/ films" APPLIED PHYSICS LETTERS, 16 MARCH 1998, AIP, USA, vol. 72, no. 11, pages 1308-1310, XP002116553 ISSN: 0003-6951 cited in the application page 1308, column 1, line 13 - line 29 -----	2

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/13787

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5292673 A	08-03-1994	JP 2816192 B	27-10-1998
		JP 3074878 A	29-03-1991
JP 10178170 A	30-06-1998	NONE	
EP 0844647 A	27-05-1998	JP 10189587 A	21-07-1998
US 5596214 A	21-01-1997	JP 2643833 B	20-08-1997
		JP 7326681 A	12-12-1995
US 3731163 A	01-05-1973	NONE	
US 5702972 A	30-12-1997	NONE	
US 5688724 A	18-11-1997	JP 6077402 A	18-03-1994

PATENT COOPERATION TREATY

02-21-02A11:05 RCVD

From the INTERNATIONAL SEARCHING AUTHORITY

To:
MYERS BIGEL SIBLEY & SAJOVEC
P.O. Box 37428
Raleigh, NC 27627
UNITED STATES OF AMERICA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing (*day/month/year*) 15/02/2002
Applicant's or agent's file reference 5347.208.WO	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 01/ 19787	International filing date (*day/month/year*) 21/06/2001
Applicant NORTH CAROLINA STATE UNIVERSITY	

1. [X] The applicant is hereby notified that the International Search Report has been established and is transmitted herewith.

Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

When? The time limit for filing such amendments is normally 2 months from the date of transmittal of the International Search Report; however, for more details, see the notes on the accompanying sheet.

Where? Directly to the International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Fascimile No.: (41-22) 740.14.35

For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no International Search Report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

[ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

[ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Further action(s):** The applicant is reminded of the following:

Shortly after **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

Within **19 months** from the priority date, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later).

Within **20 months** from the priority date, the applicant must perform the prescribed acts for entry into the national phase before all designated Offices which have not been elected in the demand or in a later election within 19 months from the priority date or could not be elected because they are not bound by Chapter II.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gennaro Cappiello

DOCKETED
By: KD
Date: 2/21/02

Form PCT/ISA/220 (July 1998)

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the PCT Applicant's Guide, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international pbulication. Furthermore, it should be emphasized that provisional protection is available in some States only.

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When?

Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How?

Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Administrative Instructions, Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped), whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international appplication is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the same time of filing the amendments with the International Bureau, also file a copy of such amendments with the International Preliminary Examining Authority (see Rule 62.2(a), first sentence).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, where upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see Volume II of the PCT Applicant's Guide.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 5347.208.WO	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, Item 5 below.	
International application No. PCT/US 01/19787	International filing date *(day/month/year)* 21/06/2001	(Earliest) Priority Date *(day/month/year)* 26/06/2000
Applicant NORTH CAROLINA STATE UNIVERSITY		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

[ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

[ ] contained in the international application in written form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readble form.

[ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

[X] the text is approved as submitted by the applicant.

[ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

[X] the text is approved as submitted by the applicant.

[ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. ______

[ ] as suggested by the applicant.

[ ] because the applicant failed to suggest a figure.

[ ] because this figure better characterizes the invention.

[X] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/19787

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/316 H01L29/51

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, PAJ, CHEM ABS Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 962 986 A (LUCENT TECHNOLOGIES INC) 8 December 1999 (1999-12-08) the whole document ---	1,4-8, 11,16,22
X	MIKHAELASHVILI V ET AL: "ELECTRICAL CHARACTERISTICS OF METAL-DIELECTRIC-METAL AND METAL- DIELECTRIC-SEMICONDUCTOR STRUCTURES BASED ON ELECTRON BEAM EVAPORATED Y2O3, TA2O5 AND AL2O3 THIN FILM" JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 84, no. 12, 15 December 1998 (1998-12-15), pages 6747-6752, XP000834966 ISSN: 0021-8979 the whole document ---	1,3,11, 15,16, 22,23

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 February 2002	15/02/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Königstein, C

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Form PCT/ISA/210 (second sheet) (July 1992)

International Application No
PCT/US 01/19787

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HARA N ET AL: "FORMATION OF AL2O3-TA2O5 DOUBLE-OXIDE THIN FILMS BY LOW-PRESSURE MOCVD AND EVALUATION OF THEIR CORROSION RESISTANCES IN ACID AND ALKALI SOLUTIONS" JOURNAL OF THE ELECTROCHEMICAL SOCIETY, ELECTROCHEMICAL SOCIETY. MANCHESTER, NEW HAMPSHIRE, US, vol. 146, no. 2, February 1999 (1999-02), pages 510-516, XP001012429 ISSN: 0013-4651 the whole document ---	1,4-8,22
X	PATENT ABSTRACTS OF JAPAN vol. 010, no. 332 (E-453), 12 November 1986 (1986-11-12) & JP 61 137370 A (TOSHIBA CORP), 25 June 1986 (1986-06-25) abstract ---	1,11,24, 34
X	US 6 060 755 A (MA YANJUN ET AL) 9 May 2000 (2000-05-09) the whole document ---	24,25, 27-32, 34,37, 39,40, 43-46
X	WO 00 01008 A (LAM RES CORP) 6 January 2000 (2000-01-06) the whole document ---	1,11
X	EP 0 816 537 A (UBE INDUSTRIES) 7 January 1998 (1998-01-07) the whole document -----	24,26

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/19787

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EP 0962986	A	08-12-1999	US	6060406 A	09-05-2000
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